Probabilistic Computing with Stochastic Magnetic Tunnel Junctions

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Digital computing is based on deterministic bits that represent 0 or 1, with stable charges on a capacitor or ferromagnets with a stable magnetic orientation. Quantum computing on the other hand is based on q-bits that represent superpositions of 0 and 1, with coherent quantities such as a single spin or the phase of a superconducting junction. Here, we draw attention to something in between, namely, a probabilistic bit or a p-bit that fluctuates between 0 and 1 that can be represented by unstable entities such as stochastic nanomagnets [1-2].

While probabilistic bits are not substitutes for *coherent* quantum bits, many applications envisioned for Noisy Intermediate Scale Quantum (NISQ) devices are shared by p-bits. Examples include hardware accelerators for combinatorial optimization and sampling problems as well as inference and learning for machine learning applications. Interestingly, a class of quantum algorithms that are used by D-Wave's quantum annealers can be represented by p-bit networks as long as the encoded system belongs to a special subclass of quantum systems that are called "stoquastic". In the absence of extreme limitations brought on by the cryogenic operation to achieve phase coherence and entanglement in quantum computers, probabilistic networks could represent more complicated stoquastic problems with fewer number of p-bits due to the flexibility of their interconnections.

Naturally, probabilistic *emulators* can be built by conventional digital computers as well. As such, it is natural to ask why dedicated hardware for probabilistic computers would be needed. Our estimates indicate that pseudorandom generators implemented in straightforward digital CMOS requires more than 100X more area compared to a mixed-signal p-bit implementation from a slightly modified 1T/1MTJ cell of the commercial STT-MRAM technology. A much lower cell area results in both better *energy-efficiency* as well as *better scaling* to build larger p-bit networks.

Recently, in a tabletop experiment [1], we demonstrated that a network of 8 p-bits that make use of such stochastic MTJs with unstable free layers can be used to solve classical optimization problems in hardware. Fig. 1a shows the 1T/1MTJ building block (p-bit) that uses the stochastic MTJs developed by the Fukami / Ohno laboratory of Tohoku University. An essential feature of this design comes from its *asynchronous* nature, namely, that there is no global clock that synchronizes the dynamical evolution of the system, rather, each p-bit is free to make an update by considering the input it receives from its neighbors. An asynchronous design that satisfies this requirement can achieve a very large number of flips per second due to the possibility of designing *massively parallel* STT-MRAM chips with more than a million 1T/1MTJ cells that operate independently.

Reference
1) Borders et al., "Integer Factorization using Stochastic Magnetic Tunnel Junctions," Nature 573, 390 (2019).
2) Camsari et al., "p-bits for Probabilistic Spin Logic", Applied Physics Reviews, 6, 1, 2019.