Co/Ni-nanowire based magnetic shift registers

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World-wide expansion of ICT infrastructures has demanded the rapid development of the markets for information storage devices. Especially, the CAGR of 40% is expected in next 5-years for the solid-solid data-storage devices which are used in various applications from smart-phones to servers in data-centers. To cover such a huge demand in the next decade however, it is needed to create novel technologies which can realize the nonvolatile memory chip having much larger bit-area-density than that of the state-of-art NAND-flash memory with the fabrication cost as same as that of the current technology.

We are interested in magnetic shift register (MSR), so called “race-track memory”,[1] as one of the candidates for the Tera-bit class nonvolatile memory fitting to the data-storage. We believe that the concept of the MSR, in which the magnetic nanowires acts as shift-register without gating elements and wires to identify spatial positions of stored data, has unique and great advantage for the purpose. The simple structure of MSR as a memory cell storing multi-bits will allow us to fabricate the memory chip with ultra-high bit-densities through the processes with acceptable costs.

From this point of view, we have been carrying out researches related to MSR which are from studies of current-induced domain wall motion (CIDWM) in nanowires to the examination of chemical vapor deposition of magnetic thin-layers as the magnetic device fabrication technique.[2-5] In this presentation we are going to show our recent experimental results on Co/Ni-nanowire based MSR’s.

The MSR’s shown in this presentation were fabricated from Co/Ni-multilayer-based stack structures prepared by using a magnetron sputtering system. We have been focusing the studies using the MSR’s on DW-position control and multi-bit read out operations. The position control of DW’s has realized by utilizing periodic width modulation for Co/Ni-nanowires.[2] The experimental results reveal that the combination of built-in potential energy valley and current-pulse-DW-driving effectively compensates DW-position fluctuation induced by CIDWM. We have also demonstrated the multi-bit read out operation utilizing a magnetic tunnel junction (MTJ) integrated on the nanowire.[3] Thanks to the Co/Pt-based synthetic antiferromagnetic structure for the reference layer of MTJ, no magnetic field was needed to achieve the data readout from the MTJ-integrated MSR.

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Reference

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3) T. Kondo *et al*., VLSI-TSA 2017.
4) Y. Ootera *et al*., APEX **8**, 113005 (2015).
5) M. Quinsat *et al*., AIP Advances **7**, 056318 (2017).