Large voltage output in CPP-MR devices using $Co_2Fe(Ga_{0.5}Ge_{0.5})$ Heusler alloy and Mg-Ti-O spacer material

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The maximum attainable voltage output ΔV_{max} ($\Delta V_{max} = J_{Bias} \times RA \times$ MR) in all-metallic current-perpendicular-to-plane giant magnetoresistance (CPP-GMR) junctions is severely limited when the CPP current density J_{Bias} exceeds certain threshold value. The MR ratio gradually decreases with increasing J_{Bias} due to the spin transfer torque (STT) that destabilizes both parallel and antiparallel magnetization configurations. One possible solution to tackle with this problem is the usage of high-resistive transparent oxide as the spacer material that suppresses the STT effect. Very recently, Nakatani *et al.*[1] reported an In-Zn-O spacer for the CPP-MR with a $Co_2(Mn_{0.6}Fe_{0.4})Ge$ Heusler compound. By properly engineering the Ag/In-Zn-O/Zn tri-layer, a large ΔV_{max} of 11.3 mV was reported in the CPP-MR devices with a bias voltage (V_B) of 70 mV. This motivates us to explore other conductive oxides as spacer materials. In this work, we report large ΔV_{max} in the CPP-GMR device with $Co_2Fe(Ga_{0.5}Ge_{0.5})$ Heusler alloy ferromagnetic layer and a high-resistive $Mg_{0.2}Ti_{0.8}O_x$ (MTO) spacer material.

We deposited the CPP-MR stack of Cr(10)/Ag(100)/CFGG(10)/Ag(1)/MTO(t_{Sp})/Ag(1)/CFGG(10)/Ag(5)/Ru(8) (thickness in nm, t_{Sp} = 2-2.5 nm) at room temperature onto a (001)MgO single-crystalline substrate. The top CFGG ferromagnetic layer was annealed at 550ºC to improve the $L2_1$ chemical order. For all the measured devices, the device resistance decreases as the bias voltage increases (**Fig. 1**), suggesting that the underlying transport mechanism is possibly spin-dependent tunneling instead of spin-dependent scattering. With 10 nm CFGG and 2.2 nm MTO, the majority of the devices show a MR ratio ranging from 15% to 25% with a *RA* of between 100 and 250 mΩ μm^2. In spite of this, several devices show large MR ratios above 30% with the maximum MR ratio of 45%. For the best device, a large ΔV_{max} of 16.2 mV was obtained at a V_B of 60 mV (**Fig. 2**), which is more than 3 times higher than the largest ΔV_{max} value of all-metallic CPP-GMR devices reported so far. Such high MR ratios were observed only thin (1 nm) Ag layers were inserted at the CFGG/MTO interfaces. The possible occurrence of current-confined-path effect will be discussed based on the microstructure characterization. The current CPP-MR result with the MTO spacer shows an advantage in view of output voltage compared to the all-metallic CPP-GMR devices, suggesting that high resistive materials hold potential to be used as the spacer layer in future read sensors of ultrahigh density magnetic recording[2] or other MR sensors that require low *RA* values.

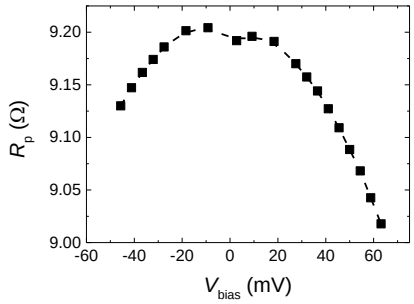

Fig. 1 Bias voltage dependence of parallel-state device resistance.

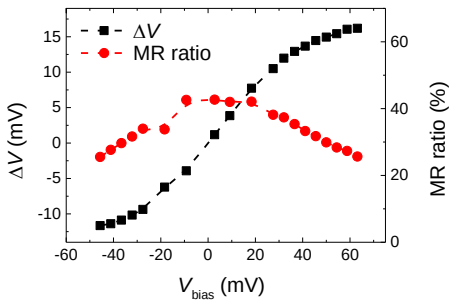

Fig. 2 Bias voltage dependence of ΔV_{max} for the best individual device.

References

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