

Fabrication of a reversal stacking of a magnetic tunnel junction by wafer bonding and thinning technique

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An MgO-based magnetic tunnel junction (MTJ) [1] is a promising candidate for use as a memory cell in spin-transfer-torque (STT) switching-type magnetoresistive random access memory (STT-MRAM). Although, our achievements have satisfied the requirements for the 30 nm generation by employing perpendicularly magnetized MTJs (p-MTJs) [2], developing a higher scalability still be an urgent issue for moving STT-MRAM on to a further generation where no one has yet practically achieved. So far, a lot of lab-level studies were made to obtain high perpendicular magnetic anisotropy (PMA) in an epitaxial film. Thanks to the high quality of the epitaxial systems, some of them such as $L1_0$ -ordered film exhibited substantially high PMA which satisfies requirements even for 1X nm generation. However, such an epitaxial under-layer is unrealistic in the STT-MRAM process because a conventional CMOS integrated wafer does not have any preferable crystal orientation. Our aim is to overcome this dilemma and merge an epitaxial film into a CMOS integrated STT-MRAM stack. In order to realize it, here we propose a new process by utilizing wafer-bonding and -sliming techniques. This process would enable us to develop an epitaxial film and a CMOS wafer individually for the benefit of the higher PMA in a film and resulting scalability in STT-MRAM. In this study, as an introductory step, we attempt these techniques for the poly-crystal film stacks. The purpose is to optimize the bonding conditions in terms of the stacking structure and the film materials.

Thin films were deposited at room temperature using a manufacturing-type sputtering apparatus (Canon-Anelva C-7100) on an 8 or 6 inches silicon wafer. Some of the MTJ samples were post-annealed at 1 hour. A wafer-bonding process was carried out at room temperature in a multi-chamber apparatus where tools for the bonding and the surface etching were equipped. In the apparatus, first the surfaces of the wafers were etched by Ar fast atom beam milling, subsequently the surfaces were put together with applying a load up to 200 kN. A wafer-thinning process was applied for as-bonded wafers. First, a coarse thinning for one back-side of the as-bonded wafers was mechanically done using grinding wheel. Then a chemical mechanical polishing was performed to remove damaged Si layer. When the rest of the wafer became 10 micron or thinner, the sample was dipped in silicon anisotropic etchant as a wet-etching process until the film element fully exposed.

In the first lot, we prepared two types of electrode stacks and applied the bonding and the thinning techniques to them. The film stacking structures are as follows: [A] Si/Si-O wafer / Ta (5 nm) / Cu-N (15 nm) / Ru (5 nm) / Ta (5 nm) / Ru-cap (20 nm). [B] Si wafer / Ta (50 nm) / Cu-N (15 nm) / Ru (5 nm) / Ta (5 nm) / Ru-cap (20 nm). For both A and B samples, the thickness of the Ru-cap was relatively thick to be 20 nm for the purpose to obtain a margin during the pre-etching (typically etching depth is 3-5 nm) in the bonding process. We planned to carry out the thinning process for the back-side of sample-B, so the thickness of the Ta buffer layer in sample-B was 10 times thicker than that of sample-A also for the margin in the final step of the thinning process. Furthermore, for the reason of the anisotropic wet-etching which does not prefer an oxide element, a bare Si wafer was employed for sample-B which was the thinning side. Figure 1 (a) and (b) show a supersonic microscopy image for the as-bonded sample and a snap of the final state of the sample, respectively. The supersonic microscopy image in (a) revealed that some part of the area were not bonded as shown in the bright contrast. It can be caused by a particle element which initially exists on a surface of a wafer. Then the photo image after thinning process in (b) reflects the result of the microscopy observation, and suggests the exposure of other layer such as Ru and Si-O besides Ta. Furthermore, peeled-like areas were seriously visible

periphery of the wafer, probably due to a scratch by contacting the wafer-mask during the film deposition process.

In the second lot, we prepared an MTJ and an electrode stack with Ta-capping as follows: [C] Si/Si-O wafer / Ta (5 nm) / Cu-N (10 nm) / Ta-cap (10 nm). [D] Si wafer / Ta (5 nm) / MTJ stack / Ta-cap (10 nm). In this series, we utilized Ta cap layers for both the samples for the comparison with Ru-capping. Figure 2 shows a cross-sectional TEM image of the bonded sample after post-annealing. It suggested that wafers were successfully bonded each other thanks to the Ta cap layers. Although some nanometer-size voids are visible at the bonding interface as bright contrasts, the frequency of them is much reduced compared to that with Ru-capping. The image also revealed that the in-plane-MTJ stack was totally remained without having an impact form a load during the bonding process. We also carried out the whole process to p-MTJ stacks [3]. Thanks to the improved pre-bonding process and the better surface smoothness for wafers, the interface showed nearly perfect bonding without any voids. Furthermore, the magnetoresistive properties (MR ratio and RA-product) and the anti-ferro coupling field of the reference layer were basically the same as the initial wafer. We confirmed that there was no deterioration in the final structure of a p-MTJ after bonding and sliming process.

In summary, we attempted wafer bonding and thinning process to the film stacks of electrodes and MTJs, and obtained the processed samples with a highly bonded interface. Finally, we successfully fabricated high quality reversal stacks of p-MTJs that showed no deterioration of the MR/RA performance.

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Reference

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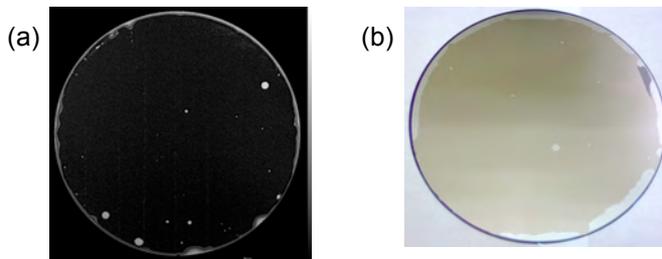


Fig.1 (a) Supersonic microscopy image of the as-bonded sample [A&B]. (b) Photo image of the sample [A&B] after thinning process.

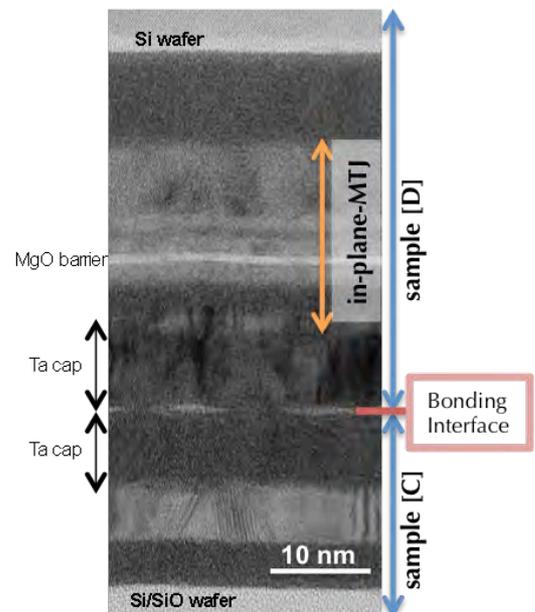


Fig.2 TEM image of an sample [C&D] after bonding process.