Low Power NV-Working Memory and NV-Logic with Spintronics/CMOS Hybrid ULSI Technology

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In information and communication technology (ICT) equipment indispensable for modern society, semiconductor memories occupy the main position of silicon storage, working memories, and logic blocks. Semiconductor memories in ICT equipment normally constitute a pyramid-like structure from cache memory (SRAM), main memory (DRAM) to storage memory (NAND). In such current semiconductor memories, there are two key issues: (1) speed gap between different levels of the memory hierarchy and (2) rapid increase in the power consumption because of the increased density. In order for ICT technology to keep contributing for the world society under the situation, where the more energy-saving is strongly required, it is essential to develop and commercialize LSIs which achieve both reduction of power dissipation and enhancement of speed performance.

In this invited talk, it is reviewed material and STT-MRAM device technology including the basics of MTJ device. Especially, our recent development results of spintronics LSIs are reviewed. We discuss STT-MRAM including the fast differential type STT-MRAM and the high-density 1T1MTJ type STT-MRAM, and then move onto MTJ based Nonvolatile (NV-) Logic LSIs. From these results, it is shown that STT-MRAM will solve both issues of speed gap and power consumption simultaneously. Next, from the background mentioned above, the directionality of the revolution in the semiconductor memory hierarchy structure is discussed. The realization of this revolution with STT-MRAMs is introduced. It is shown that our developed 1Mbit STT-MRAM fabricated with 90 nm CMOS and 70nm MTJ process, achieves Read/Write performance of 1.5nsec / 2.1nsec which is sufficient for cache memory application. Next, we show ultra-high speed 1Mbit STT-MRAM with developed differential type STT-MRAM cell (twin 1T-1MTJ cell technology), which achieves the read latency of 500 psec. Finally, NV-logic as one of application technology of leading edge memory technology is shown. It is discussed that power of MPU and Associative Processor for Image Pattern Recognition is extremely suppressed with spintronics based NV-logic technique

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