High quality cation-disorder $MgAl_2O_4$(001)-based magnetic tunnel junctions deposited by a direct sputtering technique

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Recently, the capability of $MgAl_2O_4$ tunnel barrier in magnetic tunnel junctions (MTJs) has been investigated for future non-volatile magnetoresistive memory applications. To date, large tunnel magnetoresistance (TMR) ratios exceeding 300% at room temperature (RT) were achieved in $MgAl_2O_4$-MTJs using a post-oxidation of an Mg-Al alloy layer [1]. However, the chemical inhomogeneity and interface roughness of the post-oxidized $MgAl_2O_4$ barriers have hindered the achievement of large TMR ratios for thinner barriers. In this study, we report very flat $MgAl_2O_4$ barrier interfaces with few misfit dislocations in Fe/$MgAl_2O_4$/Fe MTJs prepared by direct sputtering of a sintered $MgAl_2O_4$ target [2].

The MTJs with the following structure were prepared using a magnetron sputtering system: MgO(001) substrate/Cr (40)/Fe (100)/MgAl/$MgAl_2O_4$/Fe (7)/IrMn (12)/Ru (10), units in nm. The $MgAl_2O_4$ barrier was deposited using RF sputtering and was subsequently post-annealed at 500°C to improve the crystalline quality. The ultra-thin MgAl layer was inserted to tune the interface state. An annular dark-field scanning transmission electron microscopy (ADF-STEM) image shows the excellent quality of the barrier and perfect lattice-matched interfaces with the Fe electrodes (Fig. 1 (a)). The formation of the cation-disorder $MgAl_2O_4$ structure needed for high TMR ratios [1] was confirmed by the nano-electron beam diffraction (NBD) (inset of Fig. 1 (a)). A large TMR ratio of 245% at RT was observed, which exceeds those of epitaxial Fe/MgO/Fe (~180%) [3] and Fe/post-oxidized $MgAl_2O_4$/Fe (~212%) MTJs [4], and reflected the coherent tunneling through the half-metallic Fe-Δ_1 band. The bias voltage dependence of TMR (Fig. 1 (b)) shows that the TMR drops to the half of its zero-bias value at +1.2 V and −1.0 V, which are about two times larger than that of the MgO-based MTJs [5] and is similar to the post-oxidized $MgAl_2O_4$-based MTJs [4]. This is attributed to the high quality of the $MgAl_2O_4$ barrier with few misfit dislocations due to the perfect lattice matching with an Fe electrode. These results reveal that the direct sputtering is an alternative way for achieving high performance spinel barrier-based MTJs with uniform thin $MgAl_2O_4$ tunnel barriers.

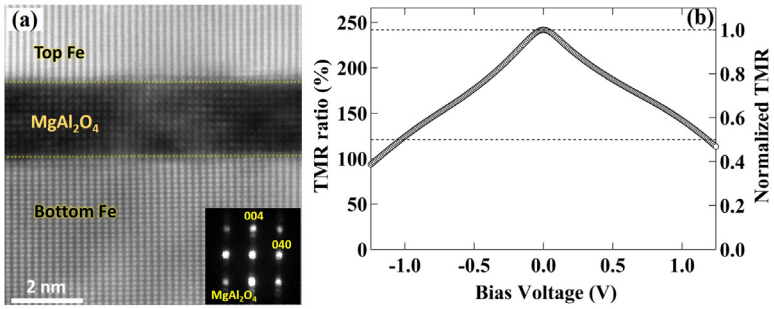

Fig. 1. (a) ADF-STEM image of an Fe/$MgAl_2O_4$ (2.10 nm)/Fe MTJ. (b) Bias voltage dependence of TMR ratio of an Fe/$MgAl_2O_4$ (1.86 nm)/Fe MTJ at RT. Inset of (a) is the NBD pattern of the barrier.

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半導体 GaO_x 障壁層を有する全単結晶トンネル磁気抵抗素子における高磁気抵抗変化率

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High magnetoresistance in fully epitaxial magnetic tunnel junctions with a semiconductor GaO_x barrier

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はじめに

スピン依存伝導に由来する磁気抵抗 (MR) 効果は、スピン電界効果トランジスタ (スピン FET) の重要な動作原理の一つである。しかしながら、通常の FET と同じ横型構造を用いた従来研究では、MR 比は室温で 0.1% 以下に留まっており、実用化に向けた大きな課題となっている。最近、金木らは高 MR 比の観点から (Ga,Mn)As/GaAs/(Ga,Mn)As 磁気トンネル接合 (MTJ) をベースとした縦型スピン FET を作製し、ゲート電圧と磁化配置に依存した出力電流の変調を極低温で観測した[1]。室温動作のためには、通常の 3*d* 磁性金属を電極として利用する必要があるため、新たに半導体障壁層材料を開発する必要がある。本研究では、近年 FET のチャネル材料として注目されている酸化ガリウム (GaO_x) を障壁層に用いた全単結晶 MTJ の開発を行った。

実験方法

膜試料は分子線エピタキシー法により MgO(001)基板上に作製された。MTJ 構造は Au(20 nm)/Co(10 nm)/Fe(5 nm)/GaO_x(1.2-2.6 nm)/MgO(0.4 nm)/Fe(30 nm) である。ここで、MgO 層は拡散防止層である。単結晶 GaO_x 膜は、蒸着直後のアモルファス膜を酸素雰囲気中アニール (500℃、1.0×10^{-7} Torr) することにより得られた。

実験結果

走査型透過電子顕微鏡像（図 1）および電子線ナノ回折像解析より、各層の結晶方位関係は、上部 Fe(001)[110] ‖ GaO_x(001)[100] ‖ MgO(001)[100] ‖ 下部 Fe(001)[110]であり、また、GaO_x は立方晶スピネル型結晶構造を有することが明らかとなった。図 2 に典型的な MR 曲線を示す。MR 比は室温 (20 K) で 94% (125%) に達し、結晶化のためのアニール未実施の素子で観測された値 (室温：34%、20 K：50%) から顕著に増大した。単結晶 MTJ で観測された MR 比はバルク Fe のスピン偏極率から予想される値を大きく上回ることから、観測された高 MR 比は、MgO[2]および MgAlO[3]障壁層を有する MTJ と同様にスピン偏極電子のコヒーレント・トンネリングに起因することが強く示唆される。本研究結果は、室温動作可能な縦型スピン FET 実現に繋がる成果である。

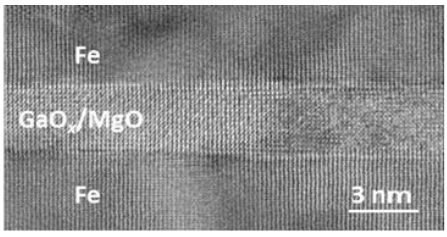

Fig.1 Cross-sessional bright-field scanning transmission electron microscopy image of the MTJ.

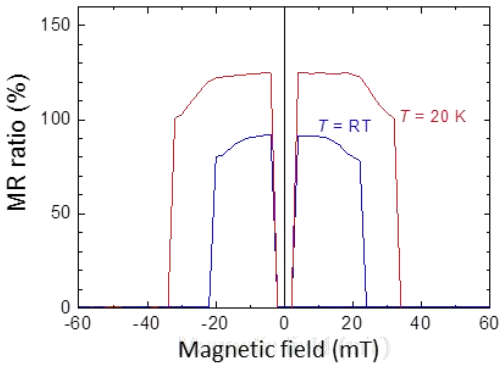

Fig.2 Magnetoresistnance curves of the MTJ at 20 K and room temperature.

謝辞

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Magnetic junctions using a $Cu(In_{0.8}Ga_{0.2})Se_2$ semiconductor spacer and $Co_2Fe(Ga_{0.5}Ge_{0.5})$ electrodes for low-resistance devices

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The discovery of large magnetoresistance (MR) effect for the magnetic tunnel junctions (MTJs) using a MgO barrier[1)] and the current-perpendicular-to-plane giant magnetoresistance (CPP-GMR) devices using Heusler alloy ferromagnetic electrodes[2)] enabled us to design the high-performance devices such as a read head sensor of the hard disk drive (HDD) over 2 Tbit/in^2 and a spin transfer torque magnetic random access memory (STT-MRAM) over gigabit class. For these applications, it is required to improve the MR ratio within an intermediate range of resistance-area-product (*RA*) from 0.1 to 1 Ω· μm^2. Therefore, many attempts have been made to reduce the *RA* values of MR devices, such as the optimization of deposition conditions of ultrathin MgO barriers in MTJs[1)] and the investigation of new metallic spacers in CPP-GMR devices[3)]. Another approach is to use a semiconducting spacer because semiconductors have smaller band gaps than the MgO (~7.8 eV). However, no promising results have been reported so far by using compound semiconductor spacers[4)]. In this study, we focused on $Cu(In_{0.8}Ga_{0.2})Se_2$ (hereafter, CIGS) compound semiconductor as a semiconductor spacer (or a barrier), the band gap of which ranges from 1.0 - 1.7 eV, having a good lattice matching with the Heusler alloys such as $Co_2Fe(Ga_{0.5}Ge_{0.5})$ (CFGG).

A film consisting of Ru(8)/Ag(5)/CFGG(10)/CIGS(2)/CFGG(10)/Ag(100)/Cr(10) (unit :nm) was deposited on a MgO (001) substrate by magnetron sputtering. After ex-situ annealing at 300°C, the film was patterned into pillars with ellipsoidal shape (0.3×0.1 μm^2) by means of electron beam lithography and Ar ion milling. Transport properties were measured by the dc-4-probe method at room temperature.

Fig. 1(a) shows the HAADF-STEM image taken from a CFGG/CIGS/CFGG tri-layer part. A well defined layered and crystalized structure with sharp interfaces is clearly observed. The CFGG and CIGS layers have the epitaxial relationship with $(001)[110]_{CFGG}$ // $(001)[110]_{CIGS}$. The CIGS layer was found to have the chalcopyrite structure, which is the low temperature phase. Moreover, the bottom and top CFGG layers were $L2_1$ and *B*2 structures, respectively. Fig. 1(b) shows the bias voltage (V_b) dependence of MR ratio and the output voltage ΔV (= MR ratio × V_b). At V_b ~ 0 mV, relatively large MR ratio of 30 % was observed. The *RA* and ΔRA values were 250 mΩ·μm^2 and 80 mΩ·μm^2, respectively. The MR ratio did not decrease obviously with increasing bias voltage. Large ΔV of 22 mV was observed at V_b = − 80 mV. These results suggest that a CIGS is a promising spacer (or barrier) material for spintronics devices where low *RA* are required.

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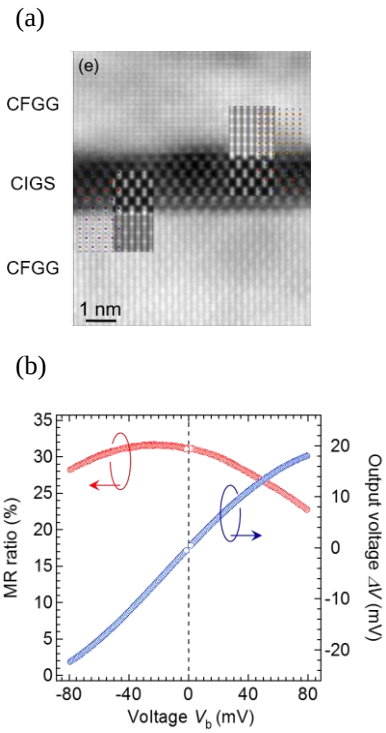

Fig.1(a) HAADF-STEM image of a CFGG/CIGS/CFGG film and (b) bias voltage dependence of MR ratio and output voltage (ΔV)

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$Mg_{1-x}Ti_xO$-based magnetic tunnel junctions with CoFeB electrodes

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The MgO-based magnetic tunnel junctions (MTJs) are the building blocks in magnetic random access memory (MRAM) [1]. Future development of gigabit-scale MRAM requires perpendicular MTJs with large tunneling magnetoresistance (TMR) ratio and resistance-area product (*RA*) lower than 10 $\Omega\mu m^2$ [2], which is very challenging for the MgO barrier considering its large band gap. Here we report on the polycrystalline MTJs using $Mg_{1-x}Ti_xO$ (x = 0.05 and 0.1) barriers that were found to show comparable TMR ratio to that of MgO-based MTJs, especially at low *RA*, and have relatively lower barrier heights.

MTJ stacks of Ta(5)/ Ru(10)/ Ta(5)/CoFeB(5)/MgO or $Mg_{1-x}Ti_xO$ (0-1.8)/ CoFeB(4)/ Ta(5)/ Ru (5, in nm) were prepared by using a magnetron sputtering system, with x = 0.05, and 0.1. The MTJ devices were fabricated by electron beam lithography, photolithography, and argon-ion milling. The MTJs were then post-annealed at 300°-450°C. The electrical measurements were performed by the four-probe method at room temperature.

The introduction of Ti into MgO was found to reduce the TMR ratio of MTJs for high *RA* range, as shown in Fig. 1. In general, the TMR ratio was found to monotonically decrease with increasing Ti concentration for the whole range of post-annealing temperature. As the *RA* decreases below 10 $\Omega\mu m^2$, the TMR ratio of MgO-based MTJs decreases rapidly and becomes lower than that of $Mg_{1-x}Ti_xO$-based MTJs (Fig. 2). Detail transmission electron microscopy (TEM) characterization found that a very thin MgO barrier have some pinholes with more dislocations at the interface while a very thin $Mg_{1-x}Ti_xO$ barrier have much less dislocations and atomically sharp interfaces. This result demonstrates the potential of $Mg_{1-x}Ti_xO$ barrier for spintronics applications that need low *RA* MTJs.

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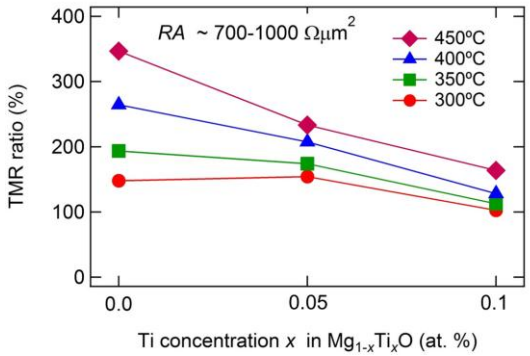

Figure 1. The TMR ratio of MgO and $Mg_{1-x}Ti_xO$-based MTJs for different post-annealing temperatures.

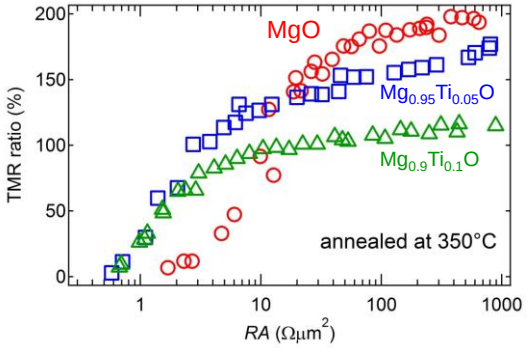

Figure 2. TMR ratio vs *RA* for MTJs post-annealed at 350°C

Enhancement of spin-dependent interfacial scattering by inserting thin NiAl layer at $Co_2Fe(Ge_{0.5}Ga_{0.5})$/Ag interface in current-perpendicular-to-plane pseudo spin valves

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All-metallic current-perpendicular-to-plane giant magnetoresistance (CPP-GMR) device have attracted much interest recently for potential applications as magnetic sensors that require low device resistance, e.g., the read sensors of high density hard disk drives. However, the main drawback of the current CPP-GMR devices is their low magnetoresistance (MR) outputs compared with those of tunneling magnetoresistance devices. A possible way to increase the MR output is to use a good band structure matched nonmagnetic (NM) spacer with half-metallic ferromagnetic (FM) layers that can generate a high spin-dependent interfacial scattering. Nakatani *et al*. reported a better band structure matching for the majority of spin electron transmittance at interface between NiAl and the $Co_2Fe(Al_{0.5}Si_{0.5})$ Heusler alloy compared to that between Ag and the Heusler alloy. However, its short spin diffusion length limited the application as a spacer layer. [1)] In order to overcome the problem of the short diffusion length, we used thin NiAl as a thin insertion layer between the Heusler alloy and spacer layers.

The pseudo spin valve (PSV) films $Co_2Fe(Ge_{0.5}Ga_{0.5})$ (10 nm)/NiAl (t_{NiAl})/Ag (5 nm)/NiAl (t_{NiAl})/$Co_2Fe(Ge_{0.5}Ga_{0.5})$ (10 nm) were prepared on Cr (10 nm)/Ag(100 nm) buffer layer that were grown on MgO (100) substrates. The thickness of the NiAl insertion layer (t_{NiAl}) was varied in the range of $0 \leq t_{NiAl} \leq 2$ nm. Fig. 1 shows the t_{NiAl} dependence of *RA*, Δ*RA*, and observed MR ratio (MR_{obs}). We confirmed a monotonic enhancement of the Δ*RA* and *RA* with increasing $t_{NiAl} \leq 0.8$ nm. However, the insertion of the NiAl layers with $t_{NiAl} \geq 1$ nm did not improve the MR output due to their short spin diffusion length. Interestingly, the insertion of 0.21 nm-thick NiAl layers at $Co_2Fe(Ge_{0.5}Ga_{0.5})$/Ag interfaces effectively improved the MR output. The highest Δ*RA* and MR ratio of 31 mΩ μm^2 and 82% at room temperature and 78 mΩ μm^2 and 285% at 10 K were obtained.[2)] These values are 2-3 times higher than those without NiAl insertion. Therefore, the $Co_2Fe(Ge_{0.5}Ga_{0.5})$/NiAl interface proposed here is expected to have a much improved spin-dependent interfacial scattering, yielding a high MR output.

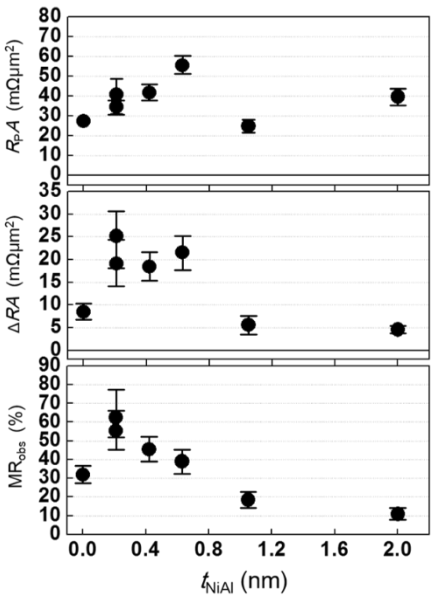

Fig. 1. The t_{NiAl} dependence of *RA*, Δ*RA*, and observed MR ratio (MR_{obs}).

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Realization of high quality epitaxial current-perpendicular-to-plane giant magnetoresistive pseudo spin-valves on Si(001) wafer using NiAl buffer layer

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Introduction

Spintronics is one of the research fields that have rapidly developed in these two decades. However, only a few applications reached to the practical level so far, i.e. there is still large gap between fundamental studies and practical applications in spintronics field. Although many previous studies on epitaxial current-perpendicular-to-plane giant magnetoresistive (CPP-GMR) devices reported excellent device performances, they are always regarded as fundamental studies because unpractical MgO single crystalline substrate is needed. In this study, we report to use NiAl buffer layer as a template for the integration of epitaxial CPP-GMR devices on a Si(001) single crystalline substrate. We confirmed by a careful microstructure analysis that the epitaxial CPP-GMR devices with half-metallic $Co_2FeGa_{0.5}Ge_{0.5}$ (CFGG) Heusler electrode grown on the buffered Si(001) substrate have a very flat and sharp interface structures. Excellent MR output that is comparable with the devices grown on an MgO(001) substrate were clearly observed in the device on Si substrate, demonstrating the possibility of epitaxial spintronic devices with NiAl template for practical applications.[1]

Experiment detail

A fully epitaxial multi-layer stack of NiAl(50)/Ag(50)/CFGG(10)/Ag(5)/CFGG(10)/Ag(5)/Ru(8) (thickness in nm) was deposited onto Si(001) single-crystalline substrates using the ultrahigh vacuum magnetron sputtering system. Crystal structure, surface roughness, magneto-resistance property and microstructure were analysed by XRD, RHEED, AFM, direct current four-probe method and TEM, respectively.

Experiment result

Figure 1 shows the stacking structure of multilayer for the whole CPP-GMR devices and the RHEED patterns for each layer. The sharp streaks in RHEED patterns for each layer demonstrate a nice epitaxial growth of CPP-GMR devices on a Si(001) single-crystalline substrate using NiAl as a buffer material. The epitaxial relationship of Si(001)[110]//NiAl(001)[110]//Ag(001)[100]//CFGG(001)[110] can be confirmed for all the layers. The usage of NiAl buffer layer successfully overcomes the difficulty of growing high quality epitaxial ferromagnetic (FM) films on Si.

Figure 2 summarizes the MR outputs of resistance change-area product (ΔRA) for the epitaxial CPP-GMR devices grown on a Si(001) substrate (red stars) as a function of annealing temperature. High magnetoresistive ratio over 27% was achieved using the CFGG Heusler alloy as ferromagnetic layers. It is important to point out that for the post-annealing temperature up to 400°C, our CPP-GMR devices grown on a Si(001) substrate presents comparable MR outputs with those grown on an MgO(001) substrate. This means we can replace the expansive impractical MgO substrate with the Si substrate to achieve high performance epitaxial CPP-GMR devices for practical sensor applications, which is a great breakthrough. More importantly, by combining this epitaxial Si/NiAl template with the wafer bonding technique,[3] various types of spintronic devices such as CPP-GMR, magnetic tunnel junctions, spin-field-effect transistors and lateral spin valves can be grown on a Si substrate and easily attached to other integrated circuits or magnetic shield layers, which is promising for next-generation spintronic applications based on epitaxial devices.

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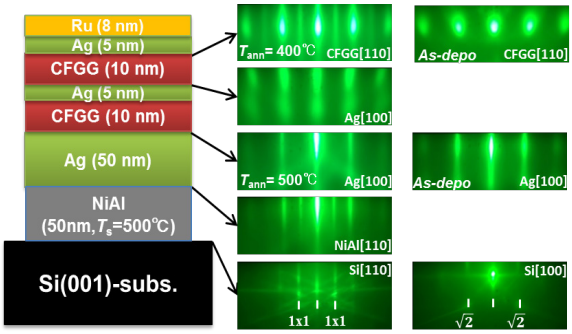

Fig.1 Structure illustration of whole CPP-GMR film stack and corresponding RHEED patterns for each layer.

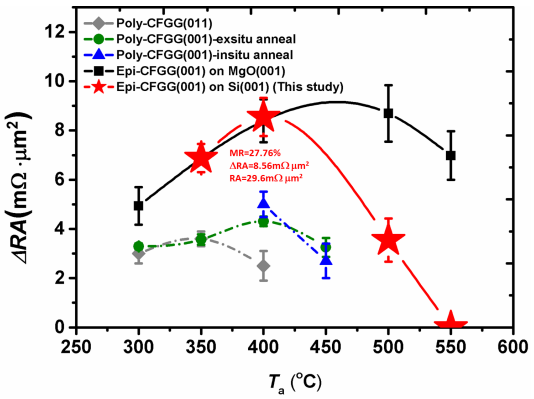

Fig.2 Annealing temperature dependence of ΔRA for various CPP-GMR devices.[2]

Fabrication of a reversal stacking of a magnetic tunnel junction by wafer bonding and thinning technique

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An MgO-based magnetic tunnel junction (MTJ) [1] is a promising candidate for use as a memory cell in spin-transfer-torque (STT) switching-type magnetoresistive random access memory (STT-MRAM). Although, our achievements have satisfied the requirements for the 30 nm generation by employing perpendicularly magnetized MTJs (p-MTJs) [2], developing a higher scalability still be an urgent issue for moving STT-MRAM on to a further generation where no one has yet practically achieved. So far, a lot of lab-level studies were made to obtain high perpendicular magnetic anisotropy (PMA) in an epitaxial film. Thanks to the high quality of the epitaxial systems, some of them such as $L1_0$-oredered film exhibited substantially high PMA which satisfies requirements even for 1X nm generation. However, such an epitaxial under-layer is unrealistic in the STT-MRAM process because a conventional CMOS integrated wafer does not have any preferable crystal orientation. Our aim is to overcome this dilemma and merge an epitaxial film into a CMOS integrated STT-MRAM stack. In order to realize it, here we propose a new process by utilizing wafer-bonding and -sliming techniques. This process would enable us to develop an epitaxial film and a CMOS wafer individually for the benefit of the higher PMA in a film and resulting scalability in STT-MRAM. In this study, as an introductory step, we attempt these techniques for the poly-crystal film stacks. The purpose is to optimize the bonding conditions in terms of the stacking structure and the film materials.

Thin films were deposited at room temperature using a manufacturing-type sputtering apparatus (Canon-Anelva C-7100) on an 8 or 6 inches silicon wafer. Some of the MTJ samples were post-annealed at 1 hour. A wafer-bonding process was carried out at room temperature in a multi-chamber apparatus where tools for the bonding and the surface etching were equipped. In the apparatus, first the surfaces of the wafers were etched by Ar fast atom beam milling, subsequently the surfaces were put together with applying a load up to 200 kN. A wafer-thinning process was applied for as-bonded wafers. First, a coarse thinning for one back-side of the as-bonded wafers was mechanically done using grinding wheel. Then a chemical mechanical polishing was performed to remove damaged Si layer. When the rest of the wafer became 10 micron or thinner, the sample was dipped in silicon anisotropic etchant as a wet-etching process until the film element fully exposed.

In the first lot, we prepared two types of electrode stacks and applied the bonding and the thinning techniques to them. The film stacking structures are as follows: [A] Si/Si-O wafer / Ta (5 nm) / Cu-N (15 nm) / Ru (5 nm) / Ta (5 nm) / Ru-cap (20 nm). [B] Si wafer / Ta (50 nm) / Cu-N (15 nm) / Ru (5 nm) / Ta (5 nm) / Ru-cap (20 nm). For both A and B samples, the thickness of the Ru-cap was relatively thick to be 20 nm for the purpose to obtain a margin during the pre-etching (typically etching depth is 3-5 nm) in the bonding process. We planned to carry out the thinning process for the back-side of sample-B, so the thickness of the Ta buffer layer in sample-B was 10 times thicker than that of sample-A also for the margin in the final step of the thinning process. Furthermore, for the reason of the anisotropic wet-etching which does not prefer an oxide element, a bare Si wafer was employed for sample-B which was the thinning side. Figure 1 (a) and (b) show a supersonic microscopy image for the as-bonded sample and a snap of the final state of the sample, respectively. The supersonic microscopy image in (a) revealed that some part of the area were not bonded as shown in the bright contrast. It can be caused by a particle element which initially exists on a surface of a wafer. Then the photo image after thinning process in (b) reflects the result of the microscopy observation, and suggests the exposure of other layer such as Ru and Si-O besides Ta. Furthermore, peeled-like areas were seriously visible

periphery of the wafer, probably due to a scratch by contacting the wafer-mask during the film deposition process.

In the second lot, we prepared an MTJ and an electrode stack with Ta-capping as follows: [C] Si/Si-O wafer / Ta (5 nm) / Cu-N (10 nm) / Ta-cap (10 nm). [D] Si wafer / Ta (5 nm) / MTJ stack / Ta-cap (10 nm). In this series, we utilized Ta cap layers for both the samples for the comparison with Ru-capping. Figure 2 shows a cross-sectional TEM image of the bonded sample after post-annealing. It suggested that wafers were successfully bonded each other thanks to the Ta cap layers. Although some nanometer-size voids are visible at the bonding interface as bright contrasts, the frequency of them is much reduced compared to that with Ru-capping. The image also revealed that the in-plane-MTJ stack was totally remained without having an impact form a load during the bonding process. We also carried out the whole process to p-MTJ stacks [3]. Thanks to the improved pre-bonding process and the better surface smoothness for wafers, the interface showed nearly perfect bonding without any voids. Furthermore, the magnetoresistive properties (MR ratio and RA-product) and the anti-ferro coupling field of the reference layer were basically the same as the initial wafer. We confirmed that there was no deterioration in the final structure of a p-MTJ after bonding and sliming process.

In summary, we attempted wafer bonding and thinning process to the film stacks of electrodes and MTJs, and obtained the processed samples with a highly bonded interface. Finally, we successfully fabricated high quality reversal stacks of p-MTJs that showed no deterioration of the MR/RA performance.

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Reference

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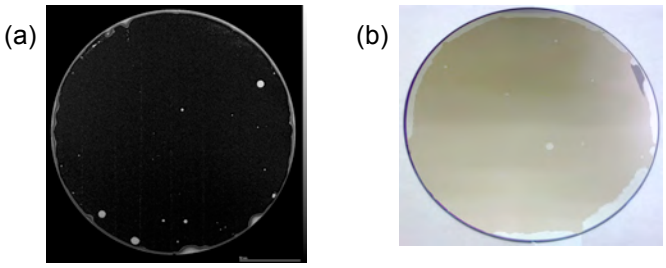

Fig.1 (a) Supersonic microscopy image of the as-bonded sample [A&B]. (b) Photo image of the sample [A&B] after thinning process.

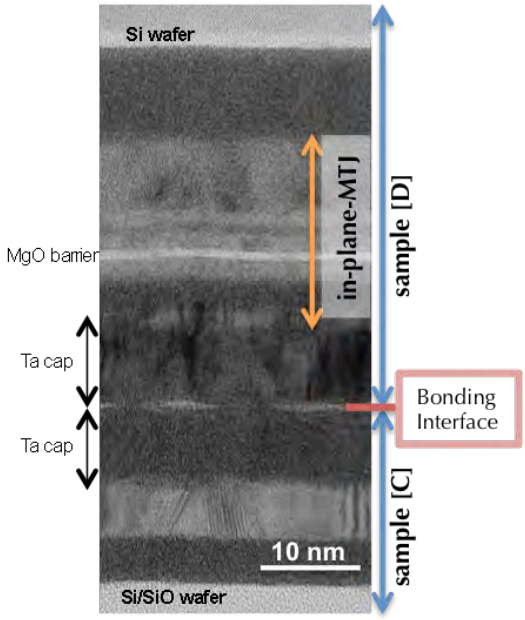

Fig.2 TEM image of an sample [C&D] after bonding process.