

Spintronics devices for nonvolatile VLSI

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Here I review two- and three-terminal nano-spintronics nonvolatile devices for VLSI integration. VLSIs can be made high performance and yet standby-power free by using nonvolatile spintronics devices ¹⁾. The most commonly employed device is magnetic tunnel junction (MTJ), a two-terminal spintronic device that can scale beyond 20 nm with perpendicular CoFeB-MgO ^{2,3)}. I will describe the development of such devices and its performance together with associated materials and physics issues. While two-terminal configuration is suitable for high density applications, three-terminal configuration allows high speed and relaxed VLSI design constraints compared to the two-terminal counterpart. Of particular interest are three-terminal devices that utilize spin-orbit torque (SOT) switching, which does not require an antiferromagnetically aligned pair of magnetic electrodes as in current-induced domain wall motion devices ⁴⁾. On this front, I will discuss high speed operation of an SOT switching device with a target ferromagnetic pillar having an out-of-plane easy axis ⁵⁾ or an in-plane magnetic easy axis collinear with the current flow direction in the underneath heavy-metal ⁶⁾. The magnetization switching is achieved with 500-ps pulses, which is not readily available in two-terminal devices utilizing spin-transfer torque (STT) switching, because STT requires switching current inversely proportional to the switching speed in this speed range. I then report the use of an antiferromagnetic material as a source of spin flow as well as the exchange field. Before, structures for fast SOT switching required a small constant external magnetic field to induce switching, which was an obstacle for application. It has been shown in a (Co/Ni)-multilayer/PtMn structure that one can switch magnetization in the absence of external magnetic field using PtMn as a source of spin ⁷⁾, removing this obstacle. I summarize my talk by comparing two- and three-terminal device performance.

This work has been carried out with S. Fukami, H. Sato, F. Matsukura, S. Ikeda, and the CSIS team, and has been supported by the ImPACT Program of CSTI (PM Dr. Masashi Sahashi) and in part by the R&D Project for ICT Key Technology of MEXT.

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Low Power NV-Working Memory and NV-Logic with Spintronics/CMOS Hybrid ULSI Technology

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In information and communication technology (ICT) equipment indispensable for modern society, semiconductor memories occupy the main position of silicon storage, working memories, and logic blocks. Semiconductor memories in ICT equipment normally constitute a pyramid-like structure from cache memory (SRAM), main memory (DRAM) to storage memory (NAND). In such current semiconductor memories, there are two key issues: (1) speed gap between different levels of the memory hierarchy and (2) rapid increase in the power consumption because of the increased density. In order for ICT technology to keep contributing for the world society under the situation, where the more energy-saving is strongly required, it is essential to develop and commercialize LSIs which achieve both reduction of power dissipation and enhancement of speed performance.

In this invited talk, it is reviewed material and STT-MRAM device technology including the basics of MTJ device. Especially, our recent development results of spintronics LSIs are reviewed. We discuss STT-MRAM including the fast differential type STT-MRAM and the high-density 1T1MTJ type STT-MRAM, and then move onto MTJ based Nonvolatile (NV-) Logic LSIs. From these results, it is shown that STT-MRAM will solve both issues of speed gap and power consumption simultaneously. Next, from the background mentioned above, the directionality of the revolution in the semiconductor memory hierarchy structure is discussed. The realization of this revolution with STT-MRAMs is introduced. It is shown that our developed 1Mbit STT-MRAM fabricated with 90 nm CMOS and 70nm MTJ process, achieves Read/Write performance of 1.5nsec / 2.1nsec which is sufficient for cache memory application. Next, we show ultra-high speed 1Mbit STT-MRAM with developed differential type STT-MRAM cell (twin 1T-1MTJ cell technology), which achieves the read latency of 500 psec. Finally, NV-logic as one of application technology of leading edge memory technology is shown. It is discussed that power of MPU and Associative Processor for Image Pattern Recognition is extremely suppressed with spintronics based NV-logic technique

This work was supported in part by CIES's Industrial Affiliation on STT -MRAM Program, R&D Project for ICT Technology of MEXT, ImPACT Program of CSTI, and ACCEL Program under JST.

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Three-terminal spintronics devices with spin-orbit torque induced switching for ultra-low power and high-performance integrated circuits

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Spintronics memory devices with three-terminal configuration are suitable for high-speed and high-reliability applications compared with the devices with two-terminal configuration, owing to their separated current paths between the read and write operations ¹⁾. Spin-orbit torque (SOT)-induced magnetization switching ^{2,3)} is a promising scheme for the write operation of the three-terminal devices. Here we show our recent studies on the SOT-induced switching which open new possibilities of the devices and integrated circuit technologies.

The previous studies on the SOT switching build on either of two structures, both of which have the magnetic easy axis of the free layer directing orthogonal to the current: perpendicular to the plane ²⁾ or in-plane and orthogonal to the channel current ³⁾. We have recently shown the third switching scheme with the easy axis collinear with the current ⁴⁾. The current-induced switching originating from the SOT with Slonczewski-like symmetry has been observed in a three-terminal device with the new structure, where a Ta/CoFeB/MgO-based stack is used. Importantly, this scheme can serve as a useful tool to investigate the physics of SOT-induced switching ⁴⁾ as well as an attractive option for the application to the integrated circuits ⁵⁾. In the presentation, we show that the new scheme allows us to unambiguously discuss the factors that determine the SOT switching current density and the difference in the dynamics between the SOT and conventional spin-transfer-torque induced magnetization switching. We also show reliable switching achieved by current pulses with the duration of 500 ps and amplitude of 1.9×10^{11} A/m²; this feature is highly promising for high-performance integrated circuits.

This work is partly supported by ImPACT Program of CSTI, R&D Project for ICT Key Technology of MEXT, and JSPS KAKENHI 15K13964 and 15J04691.

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Room temperature growth of ultrathin ordered Mn-Ga films

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$L1_0$ -MnGa alloy films have a large perpendicular magnetic anisotropy and small damping constant¹⁾ and it is potentially attractive for Spin-transfer-torque magnetoresistive random access memory (STT-MRAM) applications. Growth of ultrathin Mn-Ga films, whose thickness is usually less than 3 nm, is required for STT-switching, whereas it has been difficult.²⁻⁵⁾ Here we demonstrate the growth of ultrathin MnGa films with thickness down to 1 nm by using paramagnetic CoGa buffer layer having CsCl-type crystal structure. All the samples were prepared by a ultrahigh vacuum (UHV) magnetron sputtering system.

The sample stacking structure is MgO(001) substrate/Cr (40 nm)/CoGa (30 nm)/MnGa ($t_{\text{MnGa}}=1-5$)/Mg (0.4) /MgO (5). The Cr and CoGa buffer layers were deposited at room temperature and subsequently annealed at 700 and 500°C, respectively. The MnGa layer was deposited on the CoGa buffer layer at room temperature and not annealed. The out-of-plane polar Kerr loops for these films are shown in Fig. 1. The loops with squareness close to unity are observed even at $t_{\text{MnGa}}=1$ nm.⁶⁾ Figure 2 shows a cross-sectional image of CoGa/MnGa/MgO layers measured by a high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM). The atomically flat interfaces and well-ordered crystalline structure of the MnGa layer was observed.⁷⁾ These results indicate that the CoGa buffer layer is a promising candidate for growth of ultrathin film of Mn-based alloys. We will also discuss the spin-dependent transport properties.

This work was supported in part by NEDO, ImPACT program “Achieving ultimate Green IT Devices with long usage times without charging”, and Asahi glass foundations.

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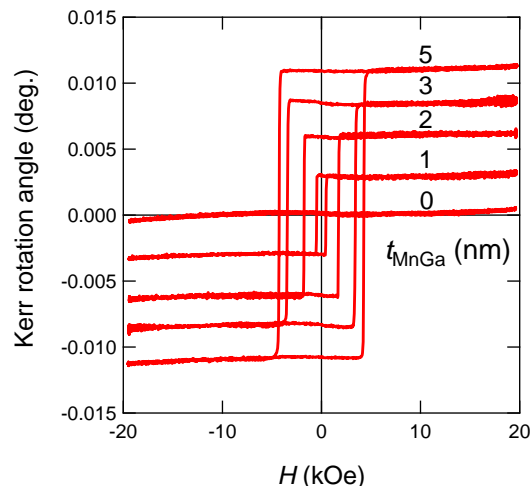


Fig. 1 Out-of-plane hysteresis curves for the ultrathin MnGa films with different thickness measured by polar magneto-optical Kerr effect.

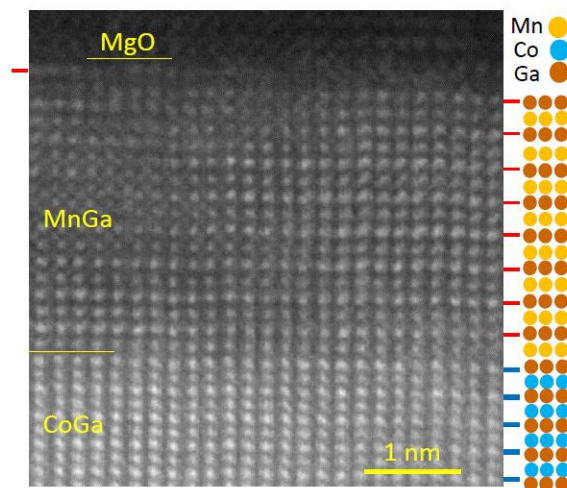


Fig.2 The cross-sectional HAADF-STEM image of the CoGa/MnGa/MgO layers. Right cartoon is the schematic for the corresponding to the atomic structures.