Voltage-Control Spintronics Memory (VoCSM) for a High-density and High-speed Non-volatile Memory

Naoharu Shimomura, Hiroaki Yoda, Tomoaki Inokuchi, Katsuhiko Koi, Yushi Kato, Altansargai Buyandalai, Satoshi Shirotori, Yuuzo Kamiguchi, Kazutaka Ikegami, Soichi Oikawa, Hideyuki Sugiyama, Mariko Shimizu, Mizue Ishikawa, Tiwari Ajay, Yuichi Ohsawa, Yoshiaki Saito, and Atsushi Kurobe
Corporate Research & Development Center, Toshiba Corporation

1 Komukai, Toshiba-cho, Saiwai-ku, Kawasaki, Kanagawa Prefecture, 212-8582, Japan

Technology to reduce energy consumption of computing devices, and especially that of working memories such as DRAM and SRAM, is critically important because of the recent drastic increase in electric power usage due to the information explosion. MRAM is the sole candidate for a non-volatile working memory because it offers the possibility of fast switching and long life time. Application of MRAM to the working memories is a focus of high expectations because of the potential advantages in terms of low-power computing.

Spin Transfer Torque (STT) has been extensively investigated as an MRAM writing scheme. However, because a same current path is used both for reading and writing, scaling and endurance are limited by read disturbance and breakdown of the tunnel barrier of MTJs, respectively. Voltage-controlled-magnetic-anisotropy (VCMA) has been proposed as the ultimate power reduction scheme. It also improves the read disturbance and the endurance. However, it requires very precise control of write pulse duration time. Meanwhile, Spin Hall writing can prevent the read disturbance because different paths are used for writing and reading. However, there is a drawback in that shrinking the cell size is difficult because it requires at least two transistors for 1 bit memory cell.

We proposed Voltage-Control Spintronics Memory (VoCSM), an architecture combining VCMA and the Spin Hall effect [1)]. As illustrated in Fig. 1, multiple (for example, 8) MTJs are aligned on a heavy metal electrode that has strong spin-orbit interaction. VoCSM handles all 8 bits simultaneously by a single write pulse. In the 1st step, all 8 bits are set to one of the 2 bit data (for example, data “zero”) by applying the voltage on the MTJs and the current pulse on the electrode. The voltage is used to lower an energy barrier between two states of the MTJs by VCMA and the current pulse gives the spin torque on the MTJs by the Spin Hall effect to switch the magnetization. After that, in the 2nd step, the opposite data (“1” in this case) is written on the selected MTJs in the 8bit memory cells depending on the data set by applying the voltage to lower or raise the energy barrier of the MTJs and also the write current pulse in the opposite direction to that of the 1st step. This writing scheme reduces the power consumption because all 8 bits are written by the single write current pulse and moreover the write current itself is reduced by VCMA. VoCSM also enables shrinking of the cell size because one MTJ requires only one transistor.

We fabricated VoCSM TEGs to prove the concept. The MTJ structure was IrMn (8nm)/ CoFe (1.8nm)/ Ru (0.9nm)/ CoFeB (1.8nm)/ MgO (1.6nm)/ (CoFeB or FeB) (1.2~2.2nm)/ electrode and the MTJ size was about 50nm×150nm. We successfully demonstrated the magnetization switching of the selected MTJs on the electrode without switching unselected ones. We also demonstrated the fast switching with 5ns write pulses which is shown in Fig. 2. The measured write error rate with 5ns writing current pulses was lower than 1×10^{-6}.

This work was funded by the ImPACT Program of the Council for Science, Technology and Innovation (Cabinet Office, Government of Japan).

Reference

1) H. Yoda et al., Digests of IEDM, 27.6 (2016).

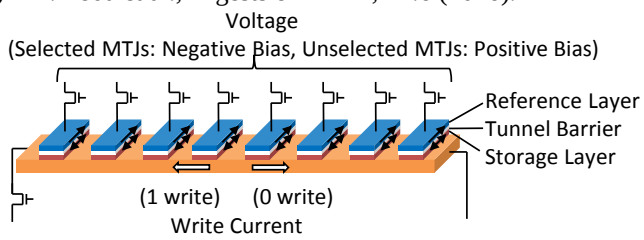

Fig. 1 Schematics of VoCSM

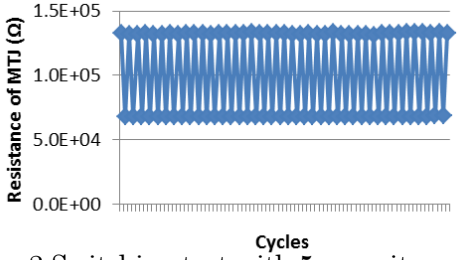

Fig. 2 Switching test with 5 ns write pulses